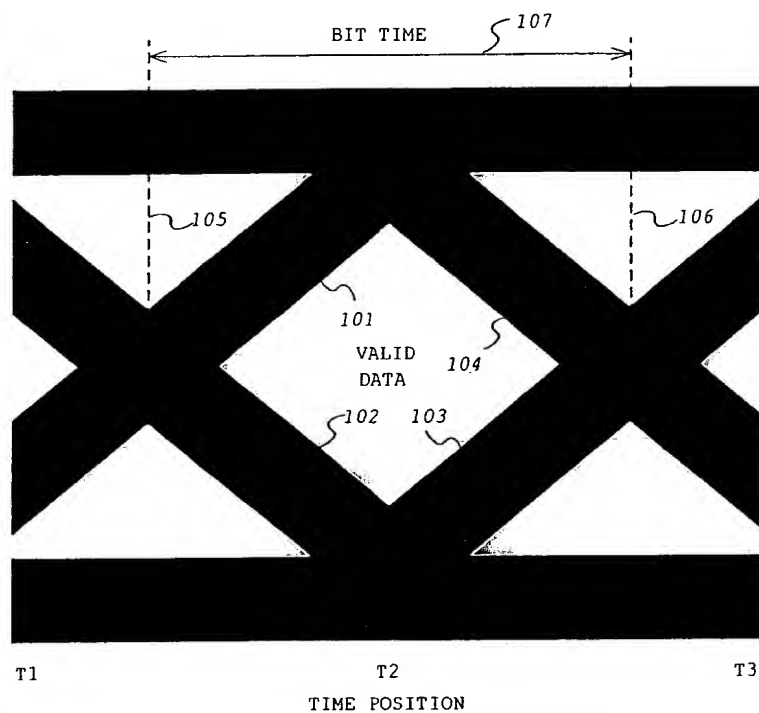
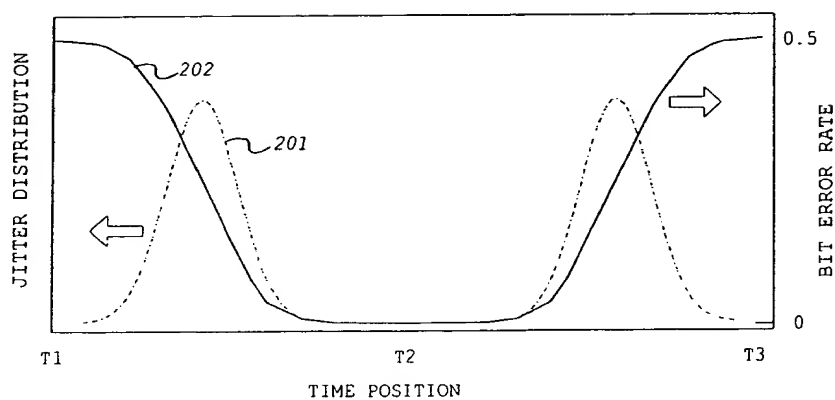


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"PRIOR ART"

FIG. 1



"PRIOR ART"

FIG. 2



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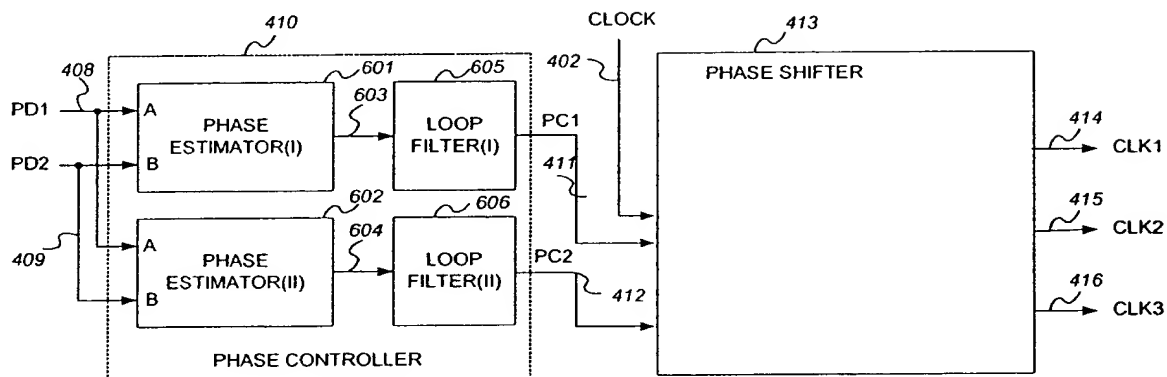
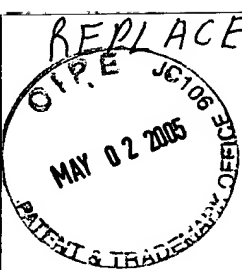


FIG. 6

The diagram illustrates a multi-stage PLL system. It begins with a 'CLOCK' input (402) entering a 'VARIABLE DELAY (I)' block (801). The output of block 801 is labeled 802 and enters a dashed box labeled 'DELAY LOCKED LOOP'. Inside this box, the signal passes through 'VARIABLE DELAY (II)' (804) and 'VARIABLE DELAY (III)' (805). A 'PHASE DETECTOR & LOOP FILTER' block (806) receives feedback from the output of block 805 (labeled 806) and provides control signals (807) to both block 804 and block 805. The output of block 805 is labeled 414 and is also the input to block 808, 'VARIABLE DELAY (IV)'. The output of block 808 is labeled 416. A 'PC1' input (411) is connected to block 801. A 'PC2' input (412) is connected to block 808. Intermediate clock outputs are labeled CLK1 (from 802), CLK2 (from 805), and CLK3 (from 808). Other labels include 401, 415, and 416.

FIG. 8



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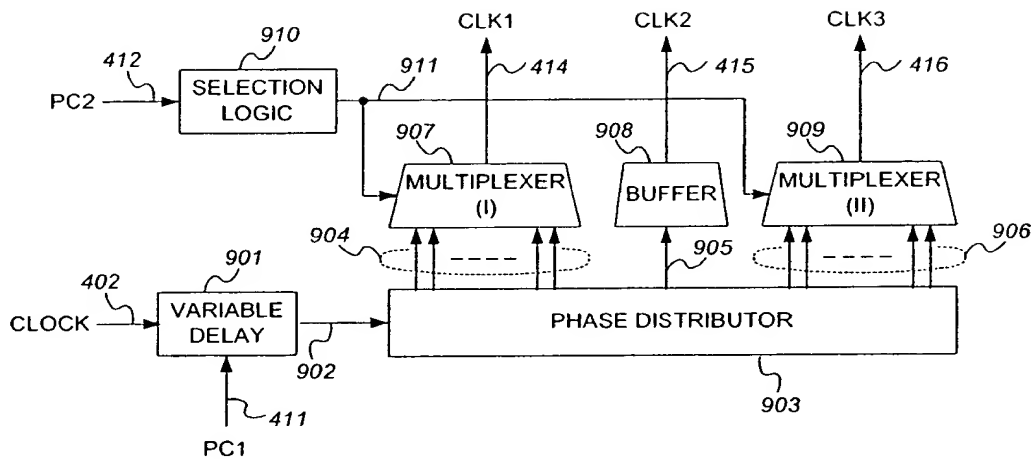


FIG. 9

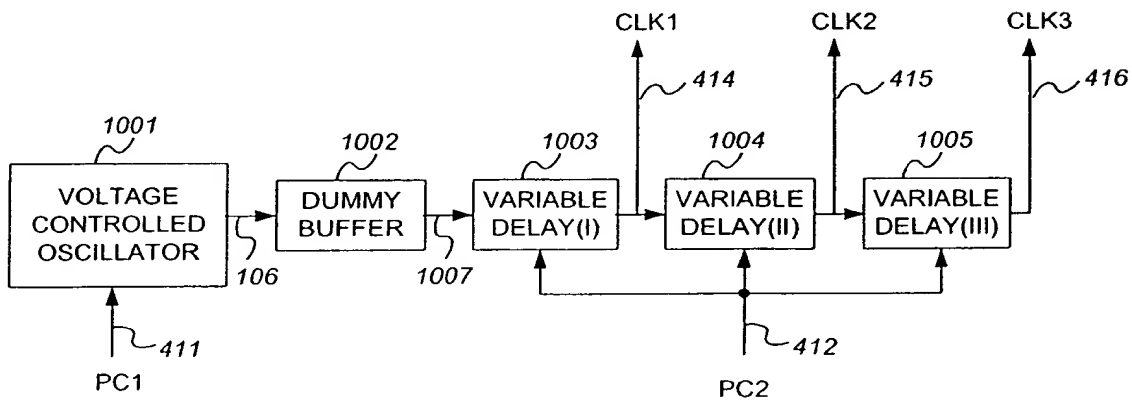


FIG. 10